Remarks

Claims 1-22 are pending in the application. By this amendment, claims 1-12, 16, and 18-22 remain in original form and claims 13-15 and 17 have been amended. In response to a restriction requirement, claims 23-31 have been canceled without prejudice as drawn to a non-elected invention.

REJECTION OF CLAIMS 1-22 UNDER 35 U.S.C. § 102(b)

Claims 1-22 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,045,490 to Esquivel et al. This rejection is respectfully traversed.

Esquivel et al. teach in column 2, lines 2-38, that a trench is formed beneath a horizontal substrate surface, the trench having at least two walls preferably separated by a bottom portion. A memory cell having a pleated floating gate is then formed in the trench. In one embodiment, the trench is n+ doped and the dopant is diffused to form source and drain electrodes along the trench walls. The bottom portion is then etched to remove the n+ substrate. Next, a dielectric layer is thermally grown along the trench walls and bottom portion. Subseqeuntly, a pleat-shaped floating gate is layered over the thermal oxide and an interlevel dielectric is formed over the floating gate. Then a control gate is deposited along the pleat-shaped floating gate.

In an alternate embodiment of the invention a nonvolatile semiconductor memory device comprises a plurality of floating gate memory cells each formed about first and second adjacent trenches on a substrate surface. A partition along the surface defines a first wall in the first trench and a second wall in the second trench. A source electrode is formed along the first wall of the first trench and a drain electrode is formed along the second wall of the second trench with a conduction channel resulting between the source and drain electrodes along an upper surface of the partition. A floating gate having at least one pleat is draped about the substrate, the floating gate substantially enveloping the electrodes and the conduction channel. A first insulative layer is interposed between the floating gate and the partition to prevent current flow between the floating gate and the electrodes and to prevent current flow between the floating gate and the conduction channel. A control gate is positioned over the floating gate, extending from the first

trench to the second trench, with a second insulative layer positioned therebetween to prevent current flow between the control gate and the floating gate.

Esquivel et al. further teach in column 4, line 45, and continuing to column 5, line 6, that a floating gate EPROM cell 50 is formed within a rectangular shaped trench beneath the horizontal surface 56 of a lightly p-doped silicon substrate 58. The trench includes two opposing side wall portions 60 and 62 separated from one another by a horizontal bottom portion 64. A pair of n+ doped source and drain electrodes 70 and 72 are formed within the trench, each along mutually opposing trench side wall portions 60 and 62. The electrodes may be formed as parts of adjacent column or bit lines according to the schematic illustration of FIG. 1 to create an array of cells 50. The memory cell 50 further comprises a pleat shaped floating gate 76 which lines the trench. As illustrated, the floating gate has one fold. However, a pleated floating gate may have multiple folds. A first dielectric layer 78, e.g., silicon oxide, isolates the floating gate 76 from the electrodes 70 and 72 and a second dielectric layer 80, e.g., a high quality gate oxide such as a thermally grown silicon oxide, is interposed between the floating gate 76 and the trench bottom portion 64. The control gate 82, also formed of polycrystalline silicon, is layered within the pleated floating gate 76 so that substrate immediately beneath the gate oxide 80 may be controlled to provide a conduction channel 84. A third dielectric layer 86 is formed between the floating gate 76 and the control gate 82. The control gate 82 extends out of the trench along the substrate surface 56 to form a portion of a row line 20.

Esquivel et al. further teach in column 6, lines 46-57, that respective source and drain electrodes associated with each cell 50 in a column 87 are connected with source and drain electrodes of other cells 50 in the same column 87 to form bit lines 88 which correspond to column lines 24 in FIG. 1. Bit line isolation is achieved either by ion implantation or trench isolation in the regions 92 which lie along columns 87 between bit lines 88 and between adjacent rows 94 of cells 50. Bit line isolation, whether by ion implantation or by trenching below the bit lines, also provides improvements in bitline to bitline punch through voltage.

Esquivel et al. teach in column 7, lines 27-64, that once the trench is formed an n+ dopant, e.g., phosphorous, is deposited and diffused into the trench (FIGS. 6b and 7b). Then an anisotropic etch is applied to selectively remove diffused n+ dopant from the trench bottom portion 64 so that isolated source and drain electrodes 70 and 72 remain along the wall portions 60 and 62 (FIGS. 6c and 7c). Next, as illustrated in FIGS. 6d and 7d, relatively thick dielectric

layers 78 are formed on the wall portions 60 and 62 and on the substrate surface 56. A layer of relatively thin gate oxide 80 is formed on the trench bottom portion. The layers 78 may be thermally grown from the exposed surfaces of the electrodes while the gate oxide is simultaneously formed from substrate on the trench bottom portion. The presence of dopant along the exposed surfaces will accelerate oxide growth causing the dielectric layers 78 to be thicker (e.g., D2=4000 Angstroms) than the gate oxide layer, (e.g., D_3=325 A). The layers 78 and the gate oxide 80 form a continuous dielectric lining along the trench interior. A first layer of doped polycrystalline semiconductor material 114 is now deposited (e.g., to 3000 Angstroms $POCl_3$ doped) over the layers 78 and gate oxide 80. See FIGS. 6e and 7e. In order to form discrete pleat-shaped floating gates 76 along the trench contour, the first polycrystalline layer 114 is pattern blocked 116 and selectively etched to preserve polycrystalline material in the trench. (FIGS. 6f and 7f). Next, in order to form the third dielectric layer 86, interlevel dielectric 118 is deposited over the entire surface, e.g., 250 Angstroms of oxide plus 150 Angstroms of nitride by low pressure chemical vapor deposition at 800 C. (FIGS. 6g and 7g) Alternatively, layer 86 may be formed by thermal oxidation along the polysilicon surface of the floating gate. A second layer of doped polysilicon 120 is then formed over the interlevel dielectric 118 filling the trench 54 and coating the entire surface.

Thus, Esquivel et al. teach building a memory element within a trench and forming the bit lines in portions of the semiconductor substrate that are adjacent the sidewalls of the trench. In other words, the bit lines are not in the trench, but in the semiconductor material adjacent the trench. Although Esquivel et al. state in column 4, lines 50-53, that a pair of n+ doped source and drain electrodes 70 and 72 are formed within the trench, each along mutually opposing trench side wall portions 60 and 62, this statement is inconsistent with the description by Esquivel et al. and the figures associated therewith. Because the term "within" means "in or into the interior" or inside, it is respectfully submitted that source and drain electrodes 70 and 72 are not inside or in the interior of the trenches. Rather, they are inside the semiconductor material and bounded by the walls of the trench. Thus, Esquivel et al. do not include, teach, or suggest a trench line, i.e., a conductive interconnect that is within a trench.

Applicant, on the other hand, teaches on page 8, lines 7-15, of the application a semiconductor substrate 300 having a surface 302 and a plurality of trenches 314 extending from surface 302 into substrate 300. A dielectric material 321 is formed in trench 314 and a trench

line 324 is formed on dielectric material 321. Polysilicon liners or inserts 336 and 338 are formed between each trench line and its corresponding trench sidewall 318. Gate structures 370 comprising gate dielectric material and a conductive material are formed on surface 302. Source regions 348 and drain regions 352 are formed in adjacent corresponding sidewalls 318. Straps or connectors 354 connect doped regions 342 to drain regions 352. Applicant further teaches on page 10, lines 5-14, that with reference to FIG. 8 a polysilicon layer 322 is planarized using, for example, a Chemical Mechanical Planarization (CMP) technique having a high selectivity to hardmask 306. Hence, the planarization stops on hardmask 306. Other suitable planarization techniques include electropolishing, electrochemical polishing, chemical polishing, and chemically enhanced polishing. After planarization, a layer of photoresist (not shown) is patterned on hardmask 306 to expose the portions of polysilicon layer 322 disposed in trenches 314. The portions of polysilicon layer 322 disposed in trenches 314 are etched using, for example, a wet etchant to form trench lines 324. By way of example, the wet etchant is dilute hydrofluoric acid (HF). Preferably, the thickness of trench lines 324, indicated by arrows 326, ranges from about 200 Å to about 2,500 Å.

Applicant teaches on page 11, lines 11-13, that with reference to FIG. 11 an undoped polysilicon layer 334 is anisotropically etched, leaving side regions or inserts 336 and 338 between sidewalls 318 and trench lines 324. Alternatively, polysilicon layer 334 is oxidized leaving inserts 336 and 338 between sidewalls 318 and trench lines 324. Because of the concentration gradient between trench lines 324 and side regions 336 and 338 and between side regions 336 and 338 and semiconductor substrate 300, the dopant in trench lines 324 diffuses through side regions 336 and 338 and into semiconductor material 300, thereby forming doped regions 342 and 344, respectively. A layer of dielectric material 346 is formed on semiconductor substrate 300, trench lines 324, the exposed portions of sidewalls 318, and on the exposed portions of side regions 336 and 338. Preferably, the formation of doped regions 342 and 344 is facilitated by forming dielectric layer 346 at temperatures sufficiently high to cause the dopant in trench lines 324 to laterally diffuse through side regions 336 and 338 and into substrate 300.

Applicant teaches on page 11, line 25, and continuing to page 12, line 12, that a dopant of N-type conductivity is implanted into semiconductor substrate 300 and trench lines 324 to form source regions 348 and to further dope source lines 324. The layer of photoresist is removed and another layer of photoresist (not shown) is patterned on dielectric layer 346 to have openings that

expose the portions of dielectric layer 346 overlying and adjacent doped regions 344. A dopant of N-type conductivity is implanted through the openings to form doped regions 350, which serve as straps or connectors that connect doped regions 344 to corresponding source regions 348. Preferably, straps 350 are formed using an angled or tilt angle implant. The layer of photoresist is removed.

Referring now to FIG. 13, a layer of photoresist (not shown) is patterned on dielectric layer 346 to have openings overlying trench lines 324 and the portions of semiconductor substrate 300 in which drain regions will be formed. It should be understood that FIG. 13 is a cross-sectional side view of the region of semiconductor substrate 300 taken along section line 13-13 of FIG. 4. A dopant of N-type conductivity is implanted into semiconductor substrate 300 and trench lines 324 to form drain regions 352 and to further dope source lines 324. The layer of photoresist is removed and another layer of photoresist (not shown) is patterned on dielectric layer 346 to have openings that expose the portions of dielectric layer 346 overlying and adjacent doped regions 342. A dopant of N-type conductivity is implanted through the openings to form doped regions 354, which serve as straps or connectors that connect doped regions 342 to corresponding drain regions 352. Preferably, straps 354 are formed using an angled or tilt angle implant.

Unlike Esquivel et al. who teach forming the bit lines in portions of the semiconductor substrate that are adjacent the sidewalls of the trench, applicant teaches that bit lines are formed from a doped semiconductor material that is deposited or formed inside the trenches. The doped semiconductor material within the trench is the trench line. Esquivel et al. do not include, teach, or suggest a trench line.

Thus applicant's claim 1 calls for, among other things, a trench line disposed in the trench, wherein the trench line is electrically coupled to the first column of memory cells. Applicant's amended claim 13 calls for, among other things, a first trench adjacent the first column of memory cells, the first trench extending into the substrate and a first trench line disposed in the first trench, wherein the source regions of the first and second memory cells are coupled to the first trench line. At least these limitations of claims 1 and 13 are not included in the relied on reference of Esquivel et al. Because all the limitations of applicant's claims 1 and 13 are not included in the relied on reference, it cannot anticipate applicant's claims 1 and 13.

Claims 2-12 depend either directly or indirectly from claim 1 and are believed allowable over the relied on reference of Esquivel et al. for at least the same reasons as claim 1. Claim 3 further sets out a first connector, wherein the first connector electrically couples one of the source region or the drain region to the trench line. Claim 4 further sets out a second connector, wherein the second connector electrically couples the other of the source region or the drain region to the trench line. Claim 5 further sets out that the trench line serves as a bit line. Claim 6 further sets out that a drain connector, wherein the drain connector electrically couples the drain region of the at least one memory cell to the trench line. Claim 7 further sets out a source connector, wherein the source connector electrically couples the source region of the at least one memory cell to the trench line. Claim 8 further sets out a source connector, wherein the source connector electrically couples the source region of the at least one memory cell to the trench line. Claim 10 further sets out another drain connector, wherein the another drain connector electrically couples the drain region of the at least one memory cell of the second column of memory cells to the trench line. Claim 11 further sets out another source connector, wherein the another source connector electrically couples the drain region of the at least one memory cell of the second column of memory cells to the trench line. At least these limitations of claims 3-8, 10, and 11 are not included in the relied on reference of Esquivel et al. further precluding anticipation of claims 3-8, 10, and 11.

Claims 14-22 depend either directly or indirectly from claim 1 and are believed allowable over the relied on reference of Esquivel et al. for at least the same reasons as claim 1. Claim 14 further sets out a second trench adjacent the first column of memory cells, the second trench extending into the substrate and a second trench line disposed in the second trench, wherein the drain regions of the first and second memory cells are coupled to the second trench line. Claim 15 further sets out a fourth memory cell having a gate structure disposed on the semiconductor substrate, a drain region, and a source region, wherein the source region of the fourth memory cell is coupled to the source region of the third memory cell and the source regions of the third and fourth memory cells are coupled to the second trench line, and wherein the third and fourth memory cells cooperate to form a second column of memory cells. Claim 16 further sets out that the second trench line is between the first and second columns of memory cells. Claim 17 further sets out a third trench adjacent the second column of memory cells, the third trench extending into the substrate and a third trench line disposed in the third trench. Claim 18 further

sets out that the drain regions of the third and fourth memory cells are coupled to the third trench line. Claim 19 further sets out that the first trench line serves as a first bit line, the second trench line serves as a second bit line, and the third trench line serves as a third bit line. At least these limitations of claims 14-19 are not included in the relied on reference of Esquivel et al. further precluding anticipation of claims 14-19.

Conclusion

No new matter is introduced by the amendments herein. Based on the foregoing, applicant believes that all claims under consideration are in condition for allowance and reconsideration of this application is respectfully requested.

Respectfully submitted,

Dated: 12 October 2005 Rennie William Dover

Rennie William Dover, Reg. No. 36,503
THE CAVANAGH LAW FIRM
1850 N. Central Avenue, Ste. 2400
Phoenix, Arizona 85004
Telephone: (602) 322-4000

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